Design and Simulation of IUPQC in Distribution System

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Abstract— In this paper a new connection for a unified power quality conditioner (UPQC) has been proposed to improve the power quality of two feeders in a distribution system. A UPQC consists of a series voltage-source converter (VSC) and a shunt VSC both joined together by a common dc bus. It is demonstrated how this device is connected between two independent feeders to regulate the bus voltage of one of the feeders while regulating the voltage across a sensitive load in the other feeder. Since the UPQC is connected between two different feeders (lines), this connection of the UPQC will be called an interline UPQC (IUPQC). The structure, control and capability of the IUPQC are discussed in this paper. The efficiency of the proposed configuration has been verified through simulation studies using MATLAB/SIMULINK.

Index Terms— Distribution system, Power quality, Sensitive load, Voltage sag, Voltage-source converter (VSC)

I. INTRODUCTION

One of the serious problems in electric systems is the increasing number of electronic components that are used by industry as well residences. These devices which we needed high quality energy to work properly, at the same, are the most responsible for injections of voltage sags, swells, harmonics and other related disturbance in the distribution system. Voltage Source Converter (VSC)-based custom power devices are increasingly being used in custom power applications for improving the power quality (PQ) of power distribution systems. Devices such as distribution static compensator (DSTATCOM) and dynamic voltage restorer (DVR) have already been discussed extensively in [1]. A DSTATCOM can compensate for distortion and unbalance in a load such that a balanced sinusoidal current flows through the feeder [2]. It can also regulate the voltage of a distribution bus [3, 4]. A DVR can compensate for voltage sag/swell and distortion in the supply side voltage such that the voltage across a sensitive/critical load terminal is perfectly regulated [5, 6]. A unified power-quality conditioner (UPQC) can perform the functions of both DSTATCOM and DVR [7, 8]. The UPQC consists of two voltage-source converters (VSCs) that are connected to a common dc bus. One of the VSCs is connected in series with a distribution feeder, while the other one is connected in shunt with the same feeder. The dc links of both VSCs are supplied through a common dc capacitor. It is also possible to connect two VSCs to two different feeders in a distribution system. In [9], a configuration called IDVR has been discussed in which two DVRs are connected in series with two separate adjacent feeders. The dc buses of the DVRs are connected together. The IDVR absorbs real power from one feeder and maintains the dc link voltage to mitigate 40% (about 0.6 p.u.) voltage sag in the other feeder with balanced loads connected in the distribution system. It is also possible to connect two shunt VSCs to different feeders through a common dc link. This can also perform the functions of the two DVRs mentioned above, albeit with higher device rating.

The UPQC consists of two voltage-source converters (VSCs) that are connected to a common dc bus. One of the VSCs is connected in series with a distribution feeder, while the other one is connected in shunt with the same feeder. The dc links of both VSCs are supplied through a common dc capacitor. It is also possible to connect two VSCs to two different feeders in a distribution system. A new connection for a UPQC called Interline UPQC (IUPQC). Two feeders, Feeder-1 and Feeder-2, which are connected to two different substations, supply the system loads L-1 and L-2. The supply voltages are denoted by V₁ and V₂ [1]. It is assumed that the IUPQC is connected to two buses B-1 and B-2, the voltages of which are denoted by V₁ and V₂ respectively. Further two feeder currents are denoted by i₁ and i₂ while the load currents are denoted by i₁ and i₂. The load L-2 voltage is denoted i₁ and i₁ by V₁ and V₂ respectively. The purpose of the IUPQC is to hold the voltages V₁ and V₂ constant against voltage sag, temporary interruption in either of the two feeders. It has been demonstrated that the IUPQC can absorb power from one feeder (say Feeder-1) to hold V₂ constant in case of a sag in the voltage V₁. This can be accomplished as the two VSCs are supplied by a common dc capacitor. The dc
capacitor voltage control has been discussed here along with voltage reference generation strategy. Also, the limits of achievable performance have been computed. The performance of the IUPQC has been evaluated through simulation studies using MATLAB/SIMULINK.

II. STRUCTURE AND CONTROL OF IUPQC

A. The IUPQC consists of two VSCs (VSC-1 and VSC-2) that are connected back to back through a common energy storage dc capacitor $C_{dc}$. Let us assume that the VSC-1 is connected in shunt to Feeder-1 while the VSC-2 is connected in series with Feeder-2. An IUPQC connected to a distribution system is shown in figure 1.

In this figure, the feeder impedances are denoted by the Pairs $(R_{s1}, L_{s1})$ and $(R_{s2}, L_{s2})$. It can be seen that the two feeders supply the loads $L-1$ and $L-2$. The load $L-1$ is assumed to have two separate components—an unbalanced part $(L-11)$ and a non-linear part $(L-12)$. The currents drawn by these two loads are denoted by $I_{L1}$ and $I_{L2}$ respectively. It is assumed that the load $L-2$ is a sensitive load that requires uninterrupted and regulated voltage. The shunt VSC (VSC-1) is connected to bus $B-1$ at the end of Feeder-1[3],[4], while the series VSC (VSC-2) is connected at bus $B-2$ at the end of Feeder-2 [5],[6]. The voltages of buses $B-1$ and $B-2$ and across the sensitive load terminal are denoted by $V_{bus}$ and $V_{L2}$ respectively. In order to attain these aims, the shunt VSC-1 is operated as a voltage controller while the series VSC-2 regulates the bus voltage $V_{bus}$ across the sensitive load [1]. The length of Feeder-1 is arbitrarily chosen to be twice that of Feeder-2.

The complete structure of a three-phase IUPQC with two such VSCs is shown in figure 2.

The secondary (distribution) sides of the shunt-connected transformers (VSC-1) are connected in star with the neutral point being connected to the load neutral. The secondary winding of the series-connected transformers (VSC-2) are directly connected in series with the bus $B-2$ and load $L-2$. The schematic structure of a VSCail is shown in Fig.4. Each of the two VSCs is realized by Three H-bridge inverters [10, 11].

In this structure, each switch represents a power semiconductor device (e.g., IGBT) and an anti-parallel diode as shown in Fig.3. All the inverters are supplied from a common single dc capacitor $C_{dc}$ and each inverter has a transformer connected at its output.

CONTROL STRATEGIES

Voltage control in inverter

Ac loads may require constant or adjustable voltage at their input terminals. When inverters feed such loads, it is essential that output voltage of the inverters is so controlled as to fulfill the requirement of ac loads. An ac load may require a constant input voltage through different levels. For such load, any variations in the dc input voltage must be suitably compensated in order to maintain a constant voltage at the load terminals at the desired level. In case inverter supplies power to a magnetic circuit, such as an induction motor the voltage to frequency ratio at the inverter output terminal must to be kept constant. This avoids saturation in the magnetic circuit of device fed by the inverter. The various methods for the control of output voltage of inverters are as under:

a) External control of ac output voltage
b) External control of dc input voltage

The first two methods require the use of peripheral components where as the third method requires no peripheral components External control of ac output voltage. There are three possible methods of external control of ac output voltage obtained from inverter output terminals. These methods are:

1. Ac voltage control
2. Series - Inverter control
3. Shunt-inverter control
1. Ac voltage controls
In this method an ac voltage controller is inserted between the output terminals of inverter and the load terminals. The voltage input the ac load is regulated through firing angle control of ac voltage controller. Is the method gives rise to higher harmonic content in the output voltage, particularly when the output voltage from the ac voltage controller is at low level. This method is therefore rarely employed expect for low power applications.

2. Series inverter control
This method of voltage control involves the use of two are more inverters in series. It illustrates how the output voltage of two inverters can be summed up with the help of transformers to obtain an adjustable output voltage, inverter output fed to two transformers whose secondary’s are connected in series, phases sum of the two fundamental voltages $V_{o1}, V_{o2}$ gives the resultant fundamental voltage $V_o$

3. Shunt inverter
Shunt control strategy involves not only generating reference current to compensate the harmonic currents but also charging the capacitor to the required value to drive the inverters. With a view to have a self-regulated dc bus, the voltage across the capacitor is sensed at regular intervals and controlled by employing a suitable closed loop control. The dc link voltage, $v_{dc}$ is sensed at a regular interval and is compared with its reference counterpart $v_{dc}^*$. The error signal is processed in a PI controller. The output of the PI controller is denoted as $I_{sp}(t)$. A limit is put on the output of controller this ensures that the source supplies active power of the load and dc bus of the UPQC. Later part of active power supplied by source is used to provide a self supported dc link of the UPQC. Thus, the dc bus voltage of the UPQC is maintained to have a proper current control [10].

4. Pulse Width Modulation Control
In this method, a fixed dc input voltage is given to the inverter and a controller ac output voltage obtained by adjusting the on and off period of the inverter components. This is the most popular method controlling the output voltage and this method is termed as Pulse Width Modulation (PWM) control.

PULSE WIDTH MODULATED INVERTERS
PWM inverters are gradually taking over other types of inverters in industrial applications. PWM techniques are characterized by constant amplitude pulses. The width of these pulses is however, modulated to obtain inverter output voltage control and to reduce its harmonic content. Different PWM techniques are as under

a) Single pulse modulation
b) Multiple pulse modulation
c) Sinusoidal pulse modulation

In PWM inverters, forced commutation is essential. The three PWM techniques listed above differ from each other in the harmonic content in their respective output voltage. Thus, choice of a particular PWM technique depends upon the permissible harmonic content in the inverter output voltages. The converter output voltage can be controlled using various control techniques. Pulse Width Modulation (PWM) techniques can be designed for the lowest harmonic content. It should be mentioned that these techniques require large number of switching per cycle leading to higher converter losses. Therefore, PWM techniques are currently considered unpractical for high voltage applications. However, it is expected that recent developments on power electronic switches will allow practical use of PWM controls on such applications in the near future. Due to their simplicity many authors, i.e. have used PWM control techniques in their UPFC studies.

SINUSOIDAL- PULSE MODULATION
When sinusoidal PWM technique is applied turn on and turn off signals for GTOs are generated comparing a sinusoidal reference signal $v_r$ of amplitude $A_r$ with a saw tooth carrier waveform $v_c$ of amplitude $A_c$. The frequency of the saw tooth waveform establishes the frequency at which GTOs are switched. The fundamental frequency of the converter output voltage is determined by the frequency of the reference signal. Controlling the amplitude of the reference signal controls the width of the pulses. The amplitude modulation index is defined as ratio of $A_c$ to $A_r$. Here $m = A_c/A_r$.

For $m \leq 1$ the peak magnitude of the fundamental frequency component of the converter Output voltage can be expressed as $V = m V_d/c/2$.

### Table I: System parameters

<table>
<thead>
<tr>
<th>System Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>System fundamental frequency</td>
<td>50Hz</td>
</tr>
<tr>
<td>Voltage source (Vs1)</td>
<td>11KV (L-Lrms), phase angle 0˚</td>
</tr>
<tr>
<td>Voltage source (Vs2)</td>
<td>11KV (L-Lrms), phase angle 0˚</td>
</tr>
<tr>
<td>Feeder-1 (Rs1+j2πfLs1)</td>
<td>Impedance : 6.05+j36.28Ω</td>
</tr>
<tr>
<td>Feeder-2 (Rs2+j2πfLs2)</td>
<td>Impedance : 3.05+j18.14Ω</td>
</tr>
<tr>
<td>Load L-11</td>
<td>Phase: a 24.2+j60.5Ω</td>
</tr>
<tr>
<td>Unbalanced RL component</td>
<td>Phase: -b 36.2+j78.54Ω</td>
</tr>
<tr>
<td>Load L-12</td>
<td>Phase: c 48.2+j94.25Ω</td>
</tr>
</tbody>
</table>

III. SYSTEM DESCRIPTION
An IUPQC connected to a distribution system is shown in Fig.1. In this figure, the feeder impedances are denoted by the pairs $(R_{s1} L_{s1})$ and $(R_{s2} L_{s2})$. It can be seen that the two feeders supply the loads L-1 and L-2. The load L-1 is assumed to have two separate components—an unbalanced part (L-1) and a non-linear part (L-12). The currents drawn by these two loads are denoted by $i_{L1}$ and $i_{L2}$.
from $\mu_1$. The reference $y_{ref}(k)$ is the desired voltage of the bus B-1. The peak of this instantaneous voltage is prespecified and its phase angle ($\delta_1$) is adjusted to maintain the power balance in the system. To set the phase angle, we note that the dc capacitor ($C_{dc}$) in (Fig. 4) must be able to supply VSC-1 while maintaining its dc bus voltage constant by drawing power from the ac system [4]

$$\delta_1 = K_p(V_{dcref} - V_{dcav})$$

(3)

Where $V_{dcav}$ is the average voltage across the dc capacitor over a cycle, $V_{dcref}$ is its set reference value and $K_p$ is the proportional gain. It is to be noted that the average voltage $V_{dcav}$ is obtained using a moving average low pass filter to eliminate all switching components from the signal. The equivalent circuit of the VSC-2 is shown in Fig. 4(b) and is similar to the one shown in Fig. 4(a) in every respect. Defining a state and input vector, respectively, as $x_2^T = [v_2\ i_2^c]$, $z_2^T = [\mu_{2c}\ i_z]$ and the state space model for VSC-2 is given as

$$x_2 = F_2x_2 + G_2z_2$$

(4)

$$y_2 = v_2 = Hx_2$$

where $F_2$ and $G_2$ are matrices that are similar to $F_1$ and $G_1$, respectively. The discrete-time input–output equivalent of (4) is given as

$$A_2(z^{-1})y_2(k) = B_2(z^{-1})\mu_{2c}(k) + C_2(z^{-1})\eta_2(k)$$

(5)

Where the disturbance $\eta_2$ is equal to $i_z$. We now use a separate pole-shift controller to determine the switching action $\mu_{2c}$ from $\mu_{2c}$. To as to track the reference signal $y_{2ref}(k)$. Note from Fig. 3 that the purpose of the VSC-2 is to hold the Voltage $V_{dc}$ across the sensitive load L-2 constant. Let us denote the reference load L-2 voltage as $V_{dcref}$. Then the reference $y_{2ref}$ is computed by the application of Kirchoff’s voltage law as [see Fig. 4(b)].

$$y_{2ref} = v_{12 - v_{12}}$$

(6)

We shall now demonstrate the normal operation of the IUPQC through simulation using MATLAB/SIMULINK. The IUPQC parameters chosen are listed in Table II and the system parameters are given in Table I. The peak of the reference voltage $y_{ref}$ is chosen as 9.0 kV and its angle is computed from the angle controller (3) with $K_p = -0.25$. The reference voltage $V_{dcref}$ is chosen as a sinusoidal waveform with a peak of 9.0 kV and a phase angle of $-10^\circ$. 

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It can be seen from Fig. 5(a), that the three-phase B-1 voltages, $v_{1b}$ are perfectly balanced with a peak of 9 kV. Once these voltages become balanced, the currents drawn by Feeder-1, $i_{a1}$ also become balanced. The load L-2 bus voltages $v_{12}$, shown in Fig. 5(c) are also perfectly sinusoidal with the desired peak of (9 kV) as the converter VSC-2 injects the required voltages in the system. Now, the performance of IUPQC has been evaluated considering various disturbance conditions. We shall also discuss and evaluate the limits of performance.

**A) Upstream Fault in Feeder-2:**

The performance of the IUPQC is tested when a fault (L-G, L-L-G, and three-phase to ground) occurs in Feeder-2 at bus B-2. The system response is shown in Fig. 13 when a 10 cycle L-G fault occurs at 0.14 s such that the a-phase of B-2 bus voltage becomes zero. When the fault occurs, the power fed to load L-2 by Feeder-2 is reduced. To meet the power requirement of the load L-2, the dc capacitor starts supplying this power momentarily. This causes the dc capacitor voltage to drop from 4.1 kV to 3.5 kV and $\delta_1$ to change from -34$^\circ$ to -42$^\circ$. It can be seen from Fig., that the L-2 load voltages remain balanced throughout the fault period. The system response is shown in Fig. 6 when a 10 cycle L-L-G fault occurs at 0.14 s such that both the a and b-phases of B-2 bus voltage become zero. B-2 bus voltages are shown in Fig. 6(a). It can be seen from Fig. 6(b), that the L-2 load voltages remain balanced. However, the dc capacitor voltage now drops to about 2.65 kV. Still it is enough to regulate both the load voltages. Now, the system performance has been tested when a three phase fault occurs at 0.14 s in Feeder-2 at bus B-2 such that the voltage $v_{12}$ becomes zero. When the fault occurs, the power fed to load L-2 by Feeder-2 becomes zero. To meet the power requirement of the load L-2, the dc capacitor starts supplying this power momentarily. This causes the dc capacitor voltage $v_{dc}$ to drop and, to offset the voltage drop, the angle $\delta_1$ retards. As a result, power is drawn from the source $V_{di}$ through Feeder-1 and supplied to both the loads L-1 and L-2. These two quantities regain their nominal steady state values once the fault is cleared. This is evident from Fig. 7.

The bus B-1 voltage $V_1$ and the load L-2 voltage $V_{12}$ are shown in Fig. 8. It can be seen that barring transients at the beginning and at the end of the fault, the voltage $V_{12}$ across the sensitive load remains balanced and sinusoidal. However, since the angle $\delta_1$ drops below -75$^\circ$, the bus B-1 voltage gets distorted and its magnitude also reduces. These voltages, however, regain their nominal values within a cycle of the removal of the fault. If the fault persists for a longer duration, the dc link voltage will continue to drop. This will gradually make the voltage tracking by either of the two VSCs impossible and both the bus B-1 and load L-2 voltages will collapse eventually. In order to avoid this, the load L-1 has to be reduced. To test this, the nonlinear load L-12 is cut off at 0.15 s when the fault occurs at 0.14 s. This implies that duration of 0.01 s is needed for the detection of the fault.

![Fig 5. System performance with an IUPQC. (a) B-1 bus voltages ($v_{1b}$), kV. (b) Feeder-1 currents ($i_{a1}$), A. (c) L-2 load voltages ($v_{12}$), kV. (d) B-2 bus voltages ($v_{12}$), kV.](image)

![Fig. 6. System response during L-L-G fault at bus B-2 (a) B-2 bus voltages($v$), kV, (b) L-2 load voltages ($v$), kV, and (c) DC Capacitor voltage($V$), kV.](image)
It is assumed that the fault is of permanent nature and source is isolated from the fault by a circuit breaker. This implies that the voltage remains zero till Feeder-2 is reenergized after repair work. It can be seen that as soon as the fault occurs, both the dc link voltage and the phase angle of B-1 bus voltage drop and, as a result, the bus B-1 voltage starts getting distorted. However, as soon as the load L-12 is cut off from the system at 0.15 s, all these quantities return to their nominal values within about three cycles.

**V. TEST SYSTEM AND SIMULATION RESULTS**

**Test System Simulation for IUPQC**

The IUPQC consists of two-voltage source converter that is connected to back-to-back through common energy storage DC capacitor. One Voltage Source Converter (VSC-1) is connected in shunt with the feeder-1 and another voltage source converter is connected in series with the other feeder-2. They have two separate load components are connected in feeder-1 i.e. unbalanced and nonlinear loads. The sensitive load is connected in feeder-2.

Test system is simulated for without and with IUPQC between two feeders in distribution system for the following cases.

1. Fault in feeder-2
   a) L-G fault
   b) L-L-G fault
   c) L-L-L-G fault
   d) L-L fault

Case (a): L-G Fault in Feeder-2

- L-G fault occurs at 0.14 sec, such that the phase-a of sensitive load bus voltage becomes zero. When the fault occurs, the power fed to load L-2 by Feeder-2 is reduced.
Case (b): L-L-G Fault

- L-L-G fault occurs between 0.14sec to 0.24sec, such that the phase-a and phase-b of sensitive load bus voltage become zero. Due to absence of IUPQC.

Case (c): L-L-L fault

- L-L-L fault occurs between 0.14sec to 0.24sec, such that magnitude of the phase-a, phase-b of sensitive load bus voltage become reduced. Due to absence of IUPQC as shown.
CONCLUSIONS

The paper illustrates the operation and control of an interline unified power quality conditioner (IUPQC). The device is connected between two feeders coming from different substations. An unbalanced and non-linear load L-1 is supplied by Feeder-1 while a sensitive load L-2 is supplied through Feeder-2. The main aim of the IUPQC is to regulate the voltage at the terminals of Feeder-1 and to protect the sensitive load from disturbances. The IUPQC discussed in the paper is capable of handling system in which the loads are unbalanced and distorted. Extensive case studies have been included to show that an IUPQC might be used as a versatile device for improving the power quality in an interconnected distribution system. In conclusion, the performance under some of the major concerns of both customer and utility e.g., harmonic contents in loads, unbalanced loads, supply voltage distortion, it has been observed that an IUPQC is able to protect the distribution system from various disturbances occurring either in Feeder-1 or in Feeder-2. As far as the common dc link voltage is at the reasonable level, the device works satisfactorily. The angle controller ensures that the real power is drawn from Feeder-1 to hold the dc link voltage Vdc constant. Therefore, even for a voltage sag or a fault in Feeder-2, VSC-1 passes real power through the dc capacitor onto VSC-2 to regulate the voltage Vdc. Finally when a fault occurs in Feeder-2 or Feeder-2 is lost, the power required by the Load L-2 is supplied through both the VSCs. This implies that the power semiconductor switches of the VSCs must be rated such that the total power transfer through them must be possible. This may increase the cost of this device.

REFERENCES