A Novel Phase Shifted DC-DC Converter with Adaptive Soft Switching to Improve Efficiency under wide Load Range

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Abstract—This paper presents a novel dc-dc converter with adaptive soft switching as a means to achieve ZVS operation for all the switches. It adopts phase shift modulation features for constant frequency operation and adaptive soft switching at low load. To accomplish this task two loops are employed; inner current control loop is to check the loading condition and turn on of auxiliary switch accordingly. Outer control loop is used to improve the dynamic performance of DC-DC converter by achieving a robust output voltage against load disturbances. This paper also presents the performance of various controllers. A 1kW/100KHz dc/dc converter is simulated and analyzed. Performance of the proposed topology is evaluated at different loads i.e. static and dynamic load (DC motor). An efficiency comparison of the converter with a reported topology has also been carried out.

Index Terms—DC-DC converter; phase-shifted; resonant tank; reverse recovery; resonant converter; Soft switching.

I. INTRODUCTION

DC-DC conversion technology has been developing very rapidly, and DC-DC converters have been widely used in industrial applications such as dc motor drives, computer systems and communication equipment. The output voltage of pulse width modulation (PWM) based DC-DC converters can be controlled by changing the duty cycle. In general, to minimize the size and weight of pulse width modulated (PWM) converters, it is required that the switching frequency must be increased [1]-[2]. However, increasing the switching frequency leads to substantial switching losses, which causes deterioration in system efficiency. Therefore, the switching losses should be reduced in the case of high switching frequency operation. Various types of resonant converters have been reported to decrease the switching losses during the transient states [3] - [5]. Numerous soft switching techniques for the switching power converters have been proposed [6] - [9]. These techniques reduce the switching losses, thus enabling high frequency operation and also reduce the overall system size.

Among many new techniques proposed for high frequency power conversion to reduce the switching loss in traditional PWM converters, the phase-shifted zero-voltage full-bridge pulse width modulation (ZVS FB-PWM) converters are most desirable since they reduce switching loss considerably without the penalty of a significant increase in conduction loss [10] - [12]. For power levels up to 3 kW, the full-bridge converters employ MOSFET switches and use Phase-Shift Modulation (PSM) to regulate the output voltage. The FB ZVS phase-shift DC-DC converter is preferred due to its remarkable features. In most of these converters, zero voltage switching (ZVS) is achieved by placing a snubber capacitor across each of the switches and either by inserting an inductor in series with the transformer or by inserting an inductor in parallel to the power transformer. These benefits can be summarized as: ZVS for all the bridge transistors, reduction of the conduction losses as compared with quasi-resonant converters, reduction of the electromagnetic noise, utilization of the device output capacitance and transformer leakage inductance, fixed-frequency operation[13] - [14]. However, there are some drawbacks as high circulating currents, loss of duty cycle, ZVS is lost for light loads i.e. narrow ZVS range and load-dependent dc characteristics, also, it undergoes various influences by ringing between the parasitic capacitor of rectifying diodes and the leakage inductance, which cause switching losses and switching noise. Since LLC resonant converter can offer wider zero voltage switching region and higher conversion efficiency, it recently has been widely adopted in the design of front end power supply where output voltage is relatively high and output load current is relatively low.

The problem of narrow ZVS range at light load current is addressed in this paper. For this an L-C-L resonant circuit, with an auxiliary active switch is employed. The main contribution of this paper is to propose a simple adaptive soft switching converter to achieve ZVS operation for all the switches. It adopts phase shift modulation features for constant frequency operation and adaptive soft switching at low load. ZVS of active switches in the lagging leg can be achieved from zero- to full-load condition. In this paper the operation of proposed full bridge phase-shifted converter and then steady state analysis of the converter is discussed in
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chapter II. Chapter III explains the design of controller. The performance at different loading condition (static and dc motor load) is analyzed in chapter IV.

II. INSIGHT INTO THE OPERATING PRINCIPLE AND CIRCUIT DESCRIPTION

Fig. 1 shows the schematic of full bridge adaptive soft switching converter and its steady state waveforms. The primary size contains five switches Q1–Q4 & Qa. The phase shifted full bridge is formed by the switches Q1–Q4 with their output parasitic capacitances C1–C4, anti-parallel diodes D1–D4. Resonant circuit is formed by resonant inductor Lr, resonant capacitor Cr, parallel inductor Lao in series with an active switch Qa, D1 & D2 are the output rectifier diodes, Lao is the output filter inductor and Cao is output filter capacitor. Vao is the output voltage reflected to primary, Vi is the input voltage, Qa=(Lr/Cr)1/2/Rao, Rao = Vao2/Po, ωo = ωa/ωv. ωa is the angular resonant frequency, ωp = 2nfs = (Lao/Cra)1/2, ωv is the angular switching frequency of converter, ωv = 2nf. The duty cycle of auxiliary switch Qa is kept low and control pulse given to the auxiliary switch depends upon the load current. The details of this current controller are discussed in chapter III.

The operation of the converter for heavy load attains ZVS for all switches but under light load, the load current is low, the ZVS of the lagging-leg switches is lost as the energy stored in the leakage inductance of the transformer is insufficient to discharge the switch and transformer capacitances. Thus, the operation of the converter for light load is discussed here. The pulse width given to switch Q1 depends upon the load current when the current reduces, pulse duration increases. Inductance in the circuit increases with turn on of Qa, so as to obtain sufficient energy to discharge the switch and transformer capacitances and hence ZVS condition at low load is obtained. Under steady state operation, eight operating states in each half switching cycle are discussed. To simplify the analysis, few assumptions made are as follows:

- All active switches and diodes are ideal.
- Inductors, capacitors and transformers used in the circuit are ideal.
- The output filter inductor, Lao is large enough so that the ripple current is neglected.
- The output filter capacitance, Cao is large enough so that the output voltage is constant.

The operation is divided into ten intervals in one cycle.

Mode 1 (t0–t1): Prior to t0 switches Q1 & Q4 are conducting and power is transferred from input to the load through switches, and rectifier diode D1. At t = t0, switch Q1 turns off with ZVS as the capacitor C1 blocks the sudden rise of the voltage across the switch. Now in this mode flow of primary current charges the output capacitance C1 of Q4 and discharges capacitor C2 of Q3. At t = t1, the voltage of C3 decreases to zero and the body diode D2 conducts naturally. This mode consists of only charge and discharge operations, it lasts a short time interval (from t0 to t1). Hence the dead time should be sufficient enough to enable this operation. In this interval the load current flows through the transformer secondary winding. Hence inductive energy provided to charge/discharge the capacitor comes from the leakage and output inductor.

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energy in the inductor. The auxiliary current flowing through the switch is given by
\[ i_a(t) = i_a(t_1) + \frac{V}{L_{al}}(t - t_1) \]  
(2)

Where, \( i_a(t_1) \) is the initial current flowing at \( t_1 \). The voltage across the switch is
\[ v_{ds3} = V \cos(\omega_r(t - t_1)) \]  
(3)

Where, \( \omega_r = 1/\sqrt{C_p(L_p + L_{r})} \) is the resonant frequency, and \( C_p = C_3 + C_e \).

**Mode 3 (t_2 - t_3):** This mode starts with the turn off of the switch \( Q_3 \), primary current flows through \( C_3 \) & \( C_e \). The capacitor \( C_3 \) begins to charge by the primary current and when voltage across \( C_3 \) becomes higher than the total voltage drop across the inductances, rectifier diode \( D_{n3} \) turns on and starts conducting and hence the secondary winding of the transformers is short circuited. Primary voltage changes from 0 to \(-V_\text{m}\). The energy required to charge the capacitor \( C_3 \) and discharge the capacitor \( C_3 \) is provided by leakage and auxiliary inductor.

\[ \frac{1}{2}(L_p + L_o)I_p^2 > \frac{1}{2}(C_p + C_r)V_i^2 \]  
(4)

Where, \( v_{ds3} \) is the voltage across the switch \( Q_3 \).

**Mode 4 (t_3 - t_4):** At the end of the mode 3, \( C_3 \) gets completely discharged, hence diode \( D_3 \) starts conducting. Primary current falls rapidly with the slope of \(-V/L_o\). Diode \( D_3 \) & \( Q_2 \) conducts during the time interval \( t_4-t_3 \) and \( Q_3 \& Q_2 \) conduct during the time interval \( t_3-t_4 \). At the end of this mode, the primary current reaches to a magnitude \(-I_p\),
\[ -\frac{di_p(t)}{dt} = \frac{V}{L_p} \quad \text{&} \quad -\frac{di_p(t-t_3)}{dt} = -\frac{v_{ds3}(t-t_3)}{L_p} \]  
(5)

Where, \( L_p = L_{pl} + L_e \).

**Mode 5 (t_4 - t_5):** Switches \( Q_3 \& Q_2 \) conduct. The power is transferred from input to the output circuit by the rectifier diode \( D_{R2} \). The current rises in the circuit and it reaches to \( I_{p-RK} \) at the end of this mode.
\[ (L_p + L_o)\frac{di_p}{dt} = V_i - \frac{V_{o'}}{R_o} \]  
(6)

From \( t_5-t_6 \) same cycle repeats for the next half cycle.

In summary since the stored energy in the auxiliary inductor is utilized additionally in lagging leg switching transition, all switching devices in the full bridge inverter of the proposed converter turn on & off with ZVS condition from no load to full load.

In order to analyze the performance of the converter in switching transition period can be expressed as:
\[ (L_p + L_o)\frac{di_p}{dt} + \frac{1}{C_e}\int i_p(t)dt = 0 \]  
(7)

Refer equation 3, at \( t=t_5 \), \( v_{ds3} = V_i \) and \( t_5 = (t_3-t_4) \)

\[ V_i = V_i \cos(\omega_r(t - t_5)) + V_i - \frac{i}{C_e \omega_r} \sin(\omega_r(t - t_5)) \]

Hence,
\[ t_4 = \frac{1}{C_e \omega_r} \tan^{-1}\left( \frac{V_i C_e \omega_r}{i_p} \right) \]  
(8)

**A. Zero Voltage Condition**

Due to the influence of energy stored in the output filter inductor, ZVS is achieved by the leading leg switches \( Q_1 \& Q_2 \) for wider range of load. For the lagging leg switches the critical current is required to attain ZVS depends on the energy stored in the inductive circuit. For the particular value of inductance the critical current required to supply sufficient inductive energy to ensure ZVS can be determined. The critical current required for the converter to attain ZVS without having any auxiliary inductance is given by,
\[ I_{p,min} = \frac{C_e}{L_{al}} V_i \]

With the incorporation of auxiliary inductor the required current will be,
\[ I_{p,min,a} = \frac{C_e}{L_{al}} V_i \]

On comparing,
\[ \frac{I_{p,min}}{I_{p,min,a}} = \sqrt{\frac{L_{al}}{L_e}} \quad \text{or} \quad I_e = \left( \frac{I_{p,min,a}}{I_{p,min}} \right)^2 L_{al} \]

Since, \( L_e = L_{al} + L_{ae} \), hence the value of auxiliary inductor required to increase the ZVS range depends on the value of ‘a’
\[ L_{ae} = (a^2 - 1)L_{al} \]  
(9)

**A. The Current Ripple**

The effective duty cycle \( d_eff \) is the ratio of the voltage pulse duration from \(+V_i\) or \(-V_i\) appearing at the transformer secondary winding in a switching cycle. The DC voltage conversion ratio of the converter directly depends upon the effective duty cycle.
\[ \alpha = \frac{V_o}{V_i} = \frac{N_{f}}{N_{p}} \quad \text{d}_{eff} \quad \text{the effective duty cycle is given by,} \]
\[ d_{eff} = d_o - \Delta d, \quad \text{where}, \quad d_o \quad \text{is the original duty cycle of the converter} \quad \text{&} \quad \Delta d \quad \text{is duty cycle loss and is given by,} \]
\[ \Delta d = \frac{I_{p} + I_{p}^2}{L_{al}} \]

**B. Dead Time**

The dead-time between the lagging leg switches is one fourth of the resonant period \((T_{R}/4)\), which is calculated by utilizing the transformer leakage inductance and the total output parasitic capacitance of the lagging leg switches. The dead-time requirement for MOSFETs is short while IGBTs require larger dead-time due to the tail current.
Hence, the dead-time requirement of the circuit must be determined based on the switching device characteristics.

### III. CONTROLLERS DESIGN

A dual loop controller is designed for the system.

#### A. Inner Loop

For adaptive control of switch $Q_a$, a current controller is designed. The principle behind the operation of this controller is that it will direct the switch only in the case of current falls to the 20% of rated current. This switch remains inoperative in the case of high load current. It will help in getting zero voltage condition from zero to the rated load condition.

![Diagram](image)

**Fig. 3.** (a) Inner Current Control loop & (b) Outer Voltage controlled loop

#### B. Outer Loop

To obtain the output voltage regulation various controllers’ i.e. PI and fuzzy controllers are discussed and later on the performance of the proposed converter using these controllers are analyzed.

**i) PI controller:** In order to design a PI controller, the linearized model of the converter has to be determined. In this, the output voltage is compared with the reference to generate the error signal and this signal is given to the PI controller to obtain the desired phase-shift for the active switches. These switches are given phase-shifted pulse to control the output voltage. The value of proportional controller, $k_p$ and integral controller, $k_i$ are taken as 0.1 and 20 and are finely tuned thereafter.

**ii) Fuzzy logic controller:** PI controller is simple to implement and easy to design, but its performance generally depends on the working point, so that the presence of parasitic elements, time-varying loads and variable supply voltages can make selection of the control parameters difficult, which ensure a proper behavior in any operating conditions. Achieving large-signal stability often calls for a reduction of the useful bandwidth, so affecting converter performance. Fuzzy control is applied to control dc–dc converters because of its simplicity, ease of design and ease of implementation. Fuzzy controllers are well suited to nonlinear time-variant systems and do not need an exact mathematical model for the system being controlled. The fuzzy logic controller determines the operating condition from the measured values and selects the appropriate control actions using the rule base created from the expert knowledge. The control will work based on two input sets: the output voltage error, $e(k) = V_{ref} - V_{dc}(k)$ and the change in error variations $de(k) = e(k) - e(k-1)$

Which are sampled at every $T_s = 5\mu s$. The $k$ is the actual sampling sequence. The basic control structure of a fuzzy logic system and its membership function for error, change in error and output are shown in Figure 4(a)-(d). The FLC has three functional blocks for calculation and two databases. The functional blocks in FLC are: 1) fuzzifier; 2) rule evaluator; and 3) defuzzifier. The two databases are Rule base and Database. Fuzzy logic uses linguistic variables instead of numerical variables. The process of converting a numerical variable (real number) into a linguistic variable (fuzzy number) is called fuzzification. For a given crisp input, fuzzifier finds the degree of membership in every linguistic variable. Since, there are only two overlapping memberships in this specific case, all linguistic variables except two will have zero membership. In FLC, the equivalent term is rules and they are linguistic in nature. A fuzzy logic controller so designed is used to control the converter by sending the desired control signal to the PWM signal generator.
IV. RESULTS AND DISCUSSION

The simulation of the 1kW, 100/50 Volt, 100 kHz full bridge phase-shifted DC/DC converter circuit is carried out. The system’s transient performance is evaluated on applying sudden load changes and the results so obtained are analysed in terms of steady state error, peak overshoot, settling time. Here two types of controllers’ i.e. PI and fuzzy controllers are discussed and the performance of the proposed converter using these controllers are analyzed.

A. At 10% of full-load to 20% of full-load

In this converter is initially loaded with 20% of the full load and then load is suddenly decreased to 10% of full-load at t=0.06 sec by step decrease in load. The output voltage and current waveform for PI Controller and Fuzzy controller are shown in fig.6.

B. At full load and 50% of load

The converter is initially full loaded and then the load is reduced suddenly to 50% of full load at t=0.06 sec. The output voltage and current are measured with this sudden change at t=0.12 sec load is again increased suddenly to full load.

C. At different values of Load Inductance, keeping resistive load constant:

The behavior of converter circuit with different values of inductive load is observed. The effect of inductance variation on output voltage is shown in fig.7.

D. Zero voltage Switching:

All the active switches in the converter turns on and off at zero voltage, so as to minimize switching losses. The voltage across drain to source at 5% of load and at full load is shown in fig. 8 (a) & (b) respectively.


V. CONCLUSION

This paper has presented two different controllers PI and fuzzy controller to improve the dynamic response of the DC/DC boost converter against the load variation. It has been observed that the system is stable from 5% of load to full load. The system shows excellent performance when DC motor load is applied. The system is also verified on full load. The system shows excellent performance when DC harvested, and the system is stable from 5% of load to 100% of load. The system shows excellent performance when DC harvested, and the system is stable from 5% of load to 100% of load.

Table I. Performance comparison between Fuzzy and PI controller

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Peak overshoot</th>
<th>Settling time (Sec)</th>
<th>% Steady state error</th>
</tr>
</thead>
<tbody>
<tr>
<td>PI controller</td>
<td>0 - 3.6</td>
<td>0 - 0.08</td>
<td>0 - 0.3</td>
</tr>
<tr>
<td>Fuzzy Controller</td>
<td>1.1 - 1.2</td>
<td>0.02</td>
<td>0.02</td>
</tr>
</tbody>
</table>

VI. REFERENCES


